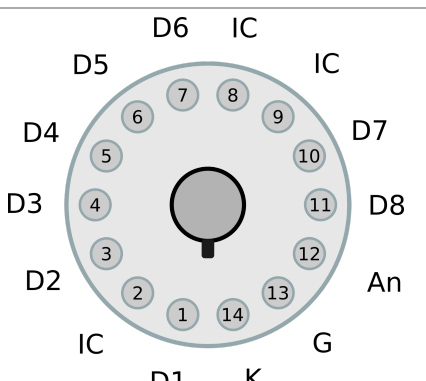
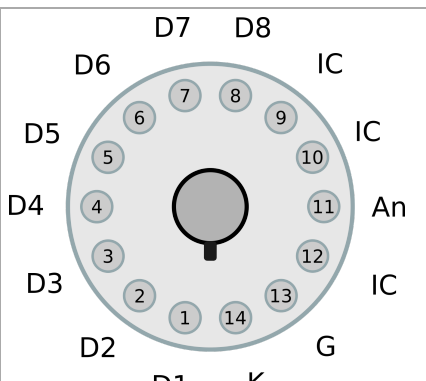
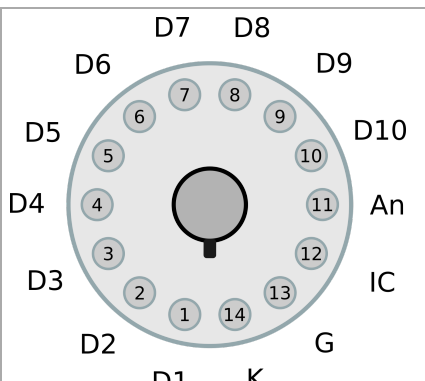




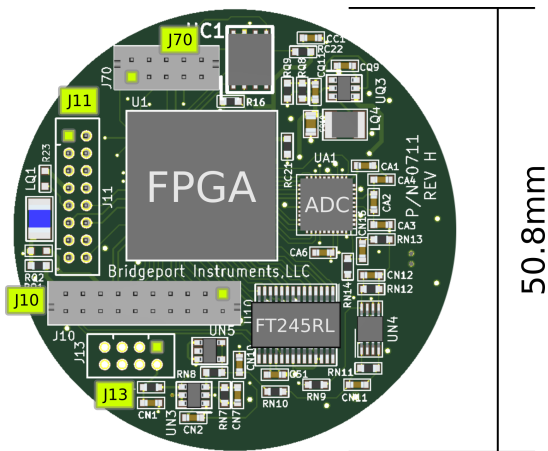
Plug-on MCA
Top, side,
bottom view.

<i>8-pin GPIO Connector, Switchcraft EN3P8MXPKG</i>		
<i>Pin</i>	<i>Function</i>	
<i>Pin</i>	<i>SEL=GND</i>	<i>SEL=3.3V or N/C</i>
1	TMS	S0
2	TDO	S2
3	TDI	S4
4	TCK	S6
5	Vref=3.3V	S7
6	VD50	
7	GND	
8	SEL	

SEL has an internal 10kΩ pull-up resistor to 3.3V. When the device is not powered via USB, it can be powered via VD50 and GND. The voltage on VD50 is +5V nominal.

<i>Three common PMT pinouts</i>		
 <p>Diagram showing 14 pins (1-14) arranged in a circle. Labels: D6, IC, IC, D7, D8, An, G, K, D1, D2, D3, D4, D5.</p>	 <p>Diagram showing 14 pins (1-14) arranged in a circle. Labels: D7, D8, IC, IC, An, IC, G, K, D1, D2, D3, D4, D5, D6.</p>	 <p>Diagram showing 14 pins (1-14) arranged in a circle. Labels: D7, D8, D9, D10, An, IC, IC, G, K, D1, D2, D3, D4, D5, D6.</p>
R6231, R6233	R1306, R1307	10-stage
P81T, N81T, P81L, N81L	P80T, N80T, P80L, N80L	P10T, N10T, P10L, N10L

Common PMT pinouts; For each pinout we show a typical PMT and the high voltage divider options.



eMorpho PCB, MCA only, no HV.

<i>Connector J70, DF11-12</i>		
#	<i>Name</i>	<i>Description</i>
1	VD33	3.3V, Vref for JTAG
2	TCK	JTAG clock
3	GND	Ground
4	TDI	JTAG Data In
5	TDO	JTAG Data Out
6	TMS	JTAG Module Select
7	C_CLK	Config Clock
8	C_CSB	Config Chip Select #
9	C_MOSI	Config MOSI
10	C_MISO	Config MISO

Pinout of the FPGA programming connector; A # indicates "active low".

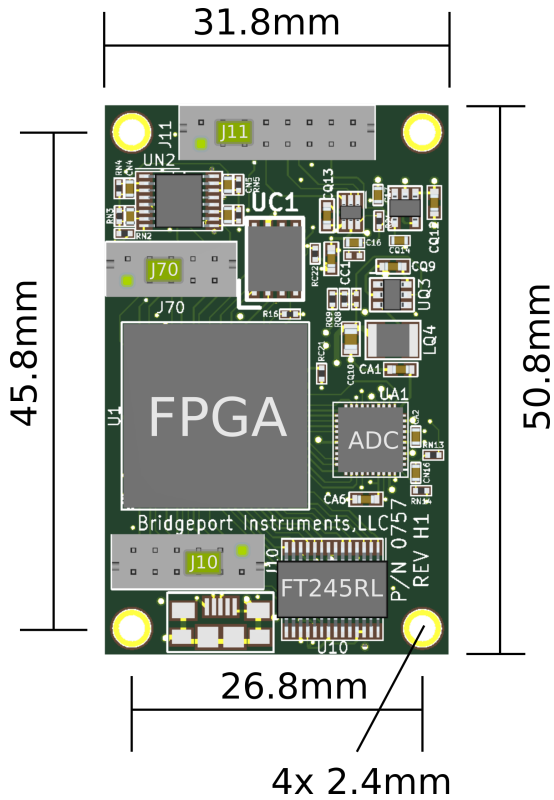
<i>Connector J10, DF11-20</i>		<i>Connector J13, DF11-8</i>	
#	<i>Name</i>	#	<i>Name</i>
1, 2, 3, 5, 6, 7, 8, 9, 11, 12, 13, 14, 16	S0 to S12	1	VD33, 3.3V out
4, 10	GND, Ground	2	Anode
15	Solder option for external input or output power	3	S11
17	5V USB power input	5, 6	S10, S12
19	USB Data –	4	Ground
20	USB Data +	7	V50; +5V from USB bus
		8	Vctrl for HV-generator

Pinout of the FPGA GPIO connector

Pinout of the secondary detector connector

<i>Connector J11, DF11-16</i>		
<i>#</i>	<i>Name</i>	<i>Description</i>
1, 7, 8, 13, 15	GND	Ground
2	An	PMT Anode
3	HV_DATA	Serial data for HV-DAC
4	VD33	3.3V supply for high voltage generator.
5	HV_CLK	Serial clock for HV-DAC
6	HV_CSB	Chip-select # for HV-DAC
9	Vctrl	Analog high voltage control
10	TC77-DATA	Serial data from TC77 temperature sensor
11	TC77-CLK	Serial clock for TC77
12	TC77-CSB	Chip-select # for TC77
14	S13	FPGA GPIO 13 or XCLK
16	S14	FPGA GPIO 14 or clock output

Pinout of the primary detector connector



slimMorpho PCB, MCA only, no HV.

<i>Connector J70, DF11-12</i>		
#	Name	Description
1	VD33	3.3V, Vref for JTAG
2	TCK	JTAG clock
3	GND	Ground
4	TDI	JTAG Data In
5	TDO	JTAG Data Out
6	TMS	JTAG Module Select
7	C_CLK	Config Clock
8	C_CSB	Config Chip Select #
9	C_MOSI	Config MOSI
10	C_MISO	Config MISO

Pinout of the FPGA programming connector; A # indicates "active low".

<i>Connector J11, DF11-16</i>		
#	Name	Description
1	USB-DM;	USB Data -
2	+5V	5V USB power input
3	USB-DP;	USB Data +
4, 5, 11, 12	GND	Ground
6	An	PMT Anode
7	HV_DATA	Serial data for HV-DAC
8	+3.3V	Output to power high voltage generator.
9	HV_CLK	Serial clock for HV-DAC
10	HV_CSB	Chip-select # for HV-DAC
13	Vctrl	Analog high voltage control
14	TC77-DATA	Serial data from TC77 temperature sensor
15	TC77-CLK	Serial clock for TC77
16	TC77-CSB	Chip-select # for TC77

Pinout of the detector and USB connector

<i>Connector J10, DF11-12</i>	
#	Name
1	V33; 3.3V out
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	S0 to S9
12	GND, Ground

Pinout of the FPGA GPIO connector